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CERTIFICATE OF TRANSMISSION

September 6, 2007

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Fax No.	:	571-273-8300
Attention	:	**EXAMINER : NADAV, ORI**
Group Unit	:	2811
From	:	Jiawei Huang, Reg. No. 43,330
MESSAGE	:	Enclosed herewith is a Supplemental Appeal Brief in 4 pages.

Sir:

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on **September 6, 2007** at the above indicated fax number.

Sign by: _____
Jiawei Huang

Application No. 09/801,350

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Examiner: NADAV, ORI

Group Art Unit: 2811

In re PATENT APPLICATION of

Applicants :	Lai et al.	)
Serial No.:	09/801,350	)
Filed:	March 07, 2001	)
For:	Electrostatic Discharge Protection Circuit Coupled On I/O Pad	)
		)

RESPONSE TO NOTIFICATION OF NON-COMPLAINT APPEAL BRIEF

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the NOTIFICATION OF NON-COMPLAINT APPEAL BRIEF dated August 08, 2007, Applicants respectfully submit the following corrected "SUMMARY OF THE CLAIMED SUBJECT MATTER" in the separate accompanying pages.

Respectfully submitted,
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Date: 9-6-2007

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V. SUMMARY OF CLAIMED SUBJECT MATTER

A conventional I/O pad ESD protection circuit comprises two transistors. When the voltage from the I/O pad is exported to an internal circuit, an ESD protection circuit usually is involved in design to prevent an over voltage from occurring and affecting the operation of the internal circuit, the two transistors can discharge electrostatic charges away when the over positive voltage or over negative voltage occur on the I/O pad. In addition, a low-voltage triggering silicon-controlled rectifier (LVTSCR) is also included, which is used to further enhance the discharge rate. However, when a current (I) supplied to the I/O pad exceeds the minimum working current (I_H) i.e. $I>I_H$, a latch-up would occur, causing the function of the ESD protection circuit to be temporarily or permanently fail.

In order to resolve the above defects of the conventional ESD protection circuit, the present inventors provide an anti-latch-up circuit (element 110 in Figure 4, lines 9-12 of page 10 of the specification), and propose to electrically connect the anti-latch-up circuit to a silicon controlled rectifier (SCR) circuit (elements 110, 104 in Figure 4, please see lines 3-6 of page 11 of the specification), which is electrically connected to the I/O pad (element 100 in Figure 4, and please see lines 13-14 of page 10 of the specification) (as recited in Claim 1). The anti-latch-up circuit is designed to prevent activation of the SCR circuit during normal IC operation (please see lines 6-8 of page 11 of the specification) (as recited in Claim 1). The SCR circuit comprises a first connection terminal (element 112 in Figure 4), a second connectional terminal (element 114 in Figure 4) and a third connectional terminal (element 116 in Figure 4, please see lines 5-6 of page 11), wherein the first connection terminal (element 112 in Figure 4) and the second connection terminal (element 114 in Figure 4) are

respectively connected to the I/O pad (element 100 in Figure 4) and a ground voltage (element GND in Figure 4) (please also see lines 13-16 of page 10); and the anti-latch-up circuit comprises a fourth connection terminal (element 126 in Figure 4), a fifth connection terminal (element 128 in Figure 4) and a sixth connection terminal (element 130 in Figure 4) respectively connected to the voltage source (element Vcc in Figure 4), the ground voltage (element GND in Figure 4) and the third connection terminal (element 116 in Figure 4) of the SCR circuit (as recited in claim 1) (please also see lines 3-6 of page 11). According to the claimed invention, the advantage of connecting the (fourth connection terminal (element 126 in Figure 4) of) anti-latch-up circuit to the voltage source and the first connection terminal (element 112 in Figure 4) of the SCR circuit to the I/O pad (element 100 in Figure 4) is that only one anti-latch-up circuit is required for several I/O pads and, therefore, the space occupation on the integrated circuit can be effectively reduced (please see line 15 of page 9 to line 2 of page 10). In other words, if the fourth connection terminal is connected to the I/O pad instead of the voltage source, then one anti-latch-up circuit is required for each of the I/O pads and thus the space occupation on the integrated circuit will be increased.

Furthermore, the present inventors propose a RC DELAY TIME of the anti-latch up circuit to be smaller than a voltage rising time of the IC power but greater than the voltage rising ESD pulse (as recited in claim 15, please also see line 17 of page 12 to line 1 of page 13). Accordingly, when there is an accidental over-voltage or voltage surge during the normal IC operation, because the RC Delay Time of the anti-latch up circuit is designed to be smaller than a voltage rising time of the IC power, therefore the rising voltage of the anti-latch-up circuit is capable of easily Out Racing the rising voltage of the rising voltage of the IC power so that a

voltage level of the node A has the same voltage (Vdd). Thus, a large amount of carriers, due to accidental over voltage, may be accordingly absorbed and the latch-up phenomenon is avoided (please see line 17 of page 12 to line 4 of page 13). On the other hand, during the ESD event, since the RC delay time of the anti-latch-up circuit is greater than the voltage rising time of the ESD pulse, therefore the rising voltage of the anti-latch-up circuit CANNOT OUT RACE the rising voltage of the ESD pulse, and therefore, the voltage level at the node A is lower compared to that of the voltage source (Vdd level), thus the SCR circuit is activated to bypass the ESD charge from the internal circuit to protect the internal circuit. Therefore the SCR circuit may be triggered at a lower holding voltage (please see line 17 of page 12 to line 4 of page 13). Thus, the anti-latch-up circuit of the present invention may be effectively utilized for effectively preventing the latching up phenomenon during the normal IC operation.